REMARKS

Claims 1, 2, 4-9, 11-13, 15-17, 19, and 20 remain pending in the instant application. All claims presently stand rejected. Reconsideration of the pending claims are respectfully requested.

Claim Rejections – 35 U.S.C. § 112

Claims 16, 17, 19, and 20 stand rejected under 35 USC § 112, first paragraph for failing to comply with the written description requirement. **The Examiner stated, "As for claim 16, the limitation 'each processor is coupled to each of the NICs' is not disclosed by the specification of the application."** Claims 17, 19, and 20 stand rejected for being dependent upon claim 16.

"An objective standard for determining compliance with the written descriptio requirement is, '**does the description clearly allow persons of ordinary skill in the art to recognize that he or she invention what is claimed.**" M.P.E.P. § 2163.02. "An applicants shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as **words**, structures, figures, diagrams, and formulas that fully set for the claimed invention." M.P.E.P. 2163.02.

Applicants respectfully disagree that claim 16 is not fully support by the originally filed specification. In fact, the specification expressly states,

> Also, in the embodiments of Figures 3 and 4, one NIC is coupled to CPUs 0-3 for the sake of clarity, but it will be understood that **embodiments of the present invention may include multiple NICs each communicatively coupled to CPUs 0-3**. (*Specification*, page 6, lines 18-21, emphasis added)

> In one embodiment, computer system 500 includes **more than one NIC, each NIC communicatively coupled to CPU 0 and CPU 1**. (*Specification*, page 11, lines 1-2, emphasis added)

The originally filed specification includes at least two instances that expressly state that embodiments include multiple NICs each communicatively coupled to multiple CPUs Accordingly, the claim language "a plurality of processors, each of the plurality of processors communicatively coupled to each of the plurality of NICs" is clearly supported by the specification and therefore satisfies the written description requirement.

Applicants request that the instant §112 rejection be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 1,2, 4, 6-9, 11-13, 15-17, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sano et al. (US 6,912,602) in view of Patterson et a . ("Computer Architecture A Quantitative Approach"). Applicants traverse the instant rejections.

Cited Prior Art Fails to Teach or Suggest All Claim Limitations

"To establish prima facie obviousness of a claimed invention, **all the claim limitations** must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

Independent claim 1 recites, in pertinent part

> wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:
> Processor Assignment = Descriptor_Position mod N,
> where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

Applicants respectfully and strenuously submit that the combination of Sano and Patterson fails to teach or suggest a striping policy that assigns a processor of a plurali y of processors to a descriptor according to the above recited relationship where 'N' is t e total number of the processors.

To be sure, the Examiner acknowledges that "[n]either of the cited references specifically discloses that the first descriptor is assigned to a processor of the plurality of processors according to the relationship of Processor assignment = Descriptor_Postio mod N" (*Office Action* mailed 4/25/06, page 6, lines 3-5). Since M.P.E.P. §2143.03 expressly requires that the prior art teach or suggest all limitation of a claim, by the Examiner own admission, the prior art of record does not establish a prima facie case f obviousness.

It appears that the Examiner is attempting to overcome the acknowledged deficient prima facie case of obviousness by making blanket statements that the missi g elements are obvious.

For example, in the Response to Arguments section, the Examiner states,

> The Examiner agrees with the Applicant that memory banks cannot be interpreted as processors. However, Sano already teaches a number of processors (see Sano, Fig. 1, Processor 12A-12N, **from which Processor assignment numbering and total number of processors (N) can be derived** ...

Office Action mailed 4/25/06, page 10, section 8. However, Sano never mentions assigning processors 12A – 12N (illustrated in FIG. 1) to descriptors 102 (illustrated i FIG. 6). Rather, Sano discloses descriptors 102 are used by packet DMA circuit 16 to implement a direct memory access of memory buffers 104 using the descriptors 102. Sano never discloses that any of processors 12 access descriptor ring 100 much less ar assigned to any of descriptors 102.

The purpose of DMA circuitry is to relieve the processor (i.e., processors 12A-12N) of the burden of memory accesses. DMA circuitry 16 is provided to execute dat transfers without using processors 12. Accordingly, not only does Sano not disclose assigning processors 12 to descriptors 102, but it teaches away from claim 1 by expressly disclosing a Packet DMA circuit 16 for accessing descriptor ring 100. See *Sano*, col. 13, line 65 through col. 14, line 30.

Similarly, Patterson does not disclose, teach, or suggest a technique for assigni g processors to descriptors. Rather, Patterson discloses a technique of interleaved mem ry including multiple memory banks where

> [t]he mapping of an address to a location in a memory bank can be expressed as two problems:
>
> Bank number = Address MOD **Number of banks**
> Address within bank = [Address/Number of banks]

Patterson, page 436. Accordingly, Patterson discloses a technique of mapping addres es to locations in memory banks—not how to assign processors to descriptors in a descriptor ring. **Since neither reference discloses assigning processors to descripto s within a descriptor ring, the cited prior art fails to constitute a prima facie case o obviousness.**

No Motivation to Combine References

Not only does the Examiner's proposed modification of the prior art fail to disclose each and every element of claim 1, but it would also render Sano unsatisfacto y for its intended purpose. "If proposed modification would render the prior art inventi n being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. M.P.E.P. § 2143.01.

Modifying Sano as suggested by the Examiner would transfer the burden of da a transfers from packet DMA circuit 16 onto processors 12, since the Examiner is proposing to assign descriptors 102 to processors 12 using a modified version of the formula "Bank number = Address MOD Number of banks" disclosed in Patterson. Ignoring that this formula does not teach or suggest assigning processors, assigning processors 12 of Sano to descriptors 102 would render DMA circuit 16 unused. This would transfer the burden of memory transfers onto processors 12. However, DMA circuit 16 is provided for the very reason to relieve processors 12 of this burden. Therefore, Sano would be rendered unsatisfactory for its intended purpose.

In fact, Sano discloses that packet DMA circuit 116 simplifies communication on the interconnect 22 for packet data transfer. See, *Sano*, col. 3, lines 44-46. Furthermo e, Sano states,

> The switch 18 may have request/grant interfaces to each of the interface circuits 20A-20C and the packet DMA circuit 16 for requesting transfers and granting those transfers. *Sano*, col. 4, lines 13-16.

The Examiner's proposed modification would reallocate the burden of data transfers from packet DMA circuit 16 onto processors 12 negating the benefit of simplified communication on interconnect 22 provided by packet DMA circuits 16. Furthermore the Examiner has not indicated how the modified circuit of Sano would operate witho t using packet DMA circuit 16 for data transfers, since the above cited portion of Sano expressly states that switch 18 interfaces directly with packet DMA circuit 16 to requ st and grant data transfers.

Impermissible Hindsight Based on Applicants Specification

Patterson clearly fails to teach or suggest "mod N" where N is a number of processors. Rather Patterson discloses "mod Number of banks". A number of memo / banks cannot reasonably be interpreted as teaching a number of processors. Similarly Sano fails to teach or suggest any sort of striping policy at all.

Accordingly, the Examiner's piecemeal combination of Patterson with Sano appears to the Applicants that the Examiner is indulging impermissible hindsight, bas d on Applicants disclosure. M.P.E.P. §2145(X)(A). It is impermissible to rearrange the parts of two references to meet the terms of a claim based on the applicants' specification. M.P.E.P. § 2144.04, subsection VI.C states,

> The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, *without the benefit of appellant's specification* to make the necessary changes in the reference device. (Emphasis added.)

(citing Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 251, 353) The Examiner combination of Sano with Patterson seems to contort both references, in addition to failing to teach or suggest each and every element.

Request for Reference or Affidavit Pursuant to MPEP § 2144.03

Since the Examiner has acknowledged that "[n]either of the cited references specifically discloses that the first descriptor is assigned to a processor of the plurality of processors according to the relationship of Processor assignment = Descriptor_Postio mod N" it appears that the Examiner is basing the rejection upon "personal knowledg or knowledge that the Examiner deems to be "well known."

In order to preserve rights, Applicants must seasonably challenge "well knowr statements" and "statements based on personal knowledge." Therefore, Applicants respectfully traverse the Examiner's assertion and request evidence in support of the Examiner's position. M.P.E.P. § 2144.03. To establish a prima facie case of obviousness, all claim limitations must be taught or suggested by the prior art. The

Examiner acknowledges his failure to cite references for all claim limitations, but relies instead on common knowledge or "well known" prior art. Therefore, Applicants respectfully request that the Examiner provide a reference or affidavit pursuant to M.P.E.P. § 2144.03 to support his assertion that it would be obvious to one of ordinary skill in the art at the time the invention was made to assign a descriptor within a descriptor ring to a processor of a plurality of processors based on the relationship: Processor assignment = Descriptor_Postion mod N, where N is a total number of the plurality of processors.

Request to Withdraw Rejections

For the above reasons, the combination of Sano and Patterson fails to teach or suggest all elements of claim 1, as required under M.P.E.P. § 2143.03. Independent claim 8, 12, and 16 include similar nonobvious elements as independent claim 1. Accordingly, Applicants request that the instant §103(a) rejections of claims 1, 8, 12, and 16 be withdrawn.

The dependent claims are nonobvious over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant § 103 rejections of the dependent claims be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

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Date: June 13, 2006

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